DT15 RECTIPTO 1.8 JAN 2005.



1204.44657X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Yasushi SHIMADA et al.

Serial No.: (not yet assigned)

Filed: Jan

January 18, 2005

For:

Multilayer Wiring Board, Manufacturing Method Thereof, Semiconductor Device, and Wireless Electronic Device

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97 & 1.98

January 18, 2005

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Sir:

In the matter of the above-identified application, applicant(s) are submitting herewith a copy of the documents listed in the attached form equivalent to Form PTO-1449 for the Examiner's consideration.

This information disclosure statement is being submitted with the new application.

To the extent that the documents listed on the attached form equivalent to Form PTO-1449 are not in the English language, the requirement of 37 CFR 1.98(a)(3) for a concise explanation of the relevance is satisfied by

an English Abstract and/or the discussion of these documents in the specification.

It is respectfully requested that this information disclosure statement be considered by the Examiner.

DT15 RC CT/PTO 18 JAN 2005

Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (1204.44657X00) and please credit any excess fees to such deposit account.

Respectfully submitted,

William I. Solomon

Registration No. 28,565

ANTONELLI, TERRY, STOUT & KRAUS, LLP

WIS/anp Attachments (703) 312-6600

PTO/SB/08A (08-03)
Approved for use through 07/31/2006. OMB 0651-0031
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STATEMENT BY APPLICANT First Named Inventor Yasushi SHIMADA et al. Art Unit Examiner Name (usa as many chapte as norpesary) Attorney Docket Number Sheet 1 of 2 1204.44657X00

U.S. PATENT DOCUMENTS						
Examiner Initials'	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		US- 5,162,977	11/10/1992	Paurus et al.		
		US- 6,265,090 B1	07/24/2001	Nishide et al.		
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FOREIGN PATENT DOCUMENTS							
Examiner Initials'	Cite No.1	Foreign Patent Document Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Τ°	
		09-148746	06/06/1997	JAPAN			
		10-013036	01/16/1998	JAPAN			
		2001-068858	03/16/2001	JAPAN			
		01-189999	07/31/1989	JAPAN			
		07-183665	07/21/1995	JAPAN			
		06-085462	03/25/1994	JAPAN			
		05-055079	03/05/1993	JAPAN			
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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

PTO/SB/08B (04-03)
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STATEMENT BY APPLICANT		First Named Inventor	Yasushi SHIMADA et al.			
				Group Art Unit		
(use as many sheets as necessary)		Examiner Name				
Sheet	2	of	2	Attorney Docket Number	1204.44657X00	

Examiner Initials*	Cite No.	NON PATENT LITERATURE DOCUMENTS Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s),	T ²
		publisher, city and/or country where published.	\vdash
		Electrical Properties of Buried Capacitor in Zero X-Y Shrinkage Multilayer Ceramic Substrate, Osama Inoue; Seiichi NAKATANI; Junichi KATO; and Yutaka TAGUCHI vol. 4, No. 2(2001) pages 145-149	
		Examination of the Built-in STO Film Capacitor Process Technology on Resin-Molded High Frequency MCM and the Capacitor Frequency Characteristics, Hiroji YAMADA and Kiichi YAMASHITA col. 4 No.7 (2001) page 590-596	
11		Integration of Thin Film Passive Circuits Using High/Low Dielectric Constant Materials, P. Chahal; A. Haridass; A. Pham; R.R. Tummala; M.G. Allen; m. Swaminathan and J. Laskar, 1997 Electronic Components and Technology Conference pages 739-744	
		National Center for Manufacturing Sciences Pages 3-1-3-6	
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Examiner	Date	
Signature	Considered	

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